Hybrid Single Electron Transistor based Low Power Consuming 4-bit Parallel Adder/Subtractor circuit in 65 nanometer technology

Sudipta Mukherjee1, Tahesin Samira Delwar2, Anindya Jana3, Subir Kumar Sarkar1

1Department of Electronics and Telecommunication Engineering, Jadavpur University, Kolkata- 700032
2Department of Electronics & Electrical Engineering, University of Science & Technology, Chittagong- 4202
3Department of Electronics & Telecommunication Engineering, University of Science & Technology, Chittagong- 4202

Abstract—Hybridization between CMOS logic and single electron transistor has already revolutionized our present nano technological aspects. Ultra low power consumption as well as ultra dense circuit formation is now possible with the help of mutual integration between the two mentioned above. These benefits have drawn the attraction of the future researchers in this hybrid SET-CMOS technology for future nano-scale low power VLSI design. In this paper, we have designed a room temperature operable 4-bit adder/subtractor circuit in hybrid SET-CMOS logic with considerably low power consumption. Power-delay product has also been calculated numerically and graphically. XOR gates are used as controlled inverter for the selection of add or subtract operation. All the simulations are performed in Tanner environment and for the simulation purpose two separate model files are used. MIB model for SET operation and BSIM4.6.1 for the operation of PMOS. It is notable that the hybrid structure provides far better performance in respect to the conventional MOSFET structure.

Keywords: MIB; BSIM4.6.1; Single Electron Transistor; 4-bit parallel adder/subtractor circuit; Hybrid SET-CMOS.

I. INTRODUCTION

Downscaling of MOSFETs has led towards denser circuits with low power consumption. But some operational hindrances [1] like short channel effects have invoked in consequences to them. Therefore urgent need for new technologies to meet our industrial requirements appeared. Single electron transistor [2] is such a nano dimensional device where one by one electron passes due to the effect of quantum mechanical tunnelling. This device is now hybridized [3] with conventional CMOS logic to extract both of their advantages in a single track by mutual integration.

II. SINGLE ELECTRON TRANSISTOR

Single electron transistor comprises of a nano-dimensional mesoscopic (conductive/semiconducting) island [Quantum Dot] having ultra-low capacitance value connected with source and drain contacts placing very high resistive, nearly 1 nm. thick tunnel junction of in between them and maintaining capacitive coupling to the gate electrode. Following fig.1 shows that.

Quantum dot being nano-dimensional, can be assumed as a quantum well having two barrier layers of finite energy height at each of its sides. Similar to the renowned ‘Particle in a Box’ concept where energy, \( E = n^2 \hbar^2 \pi^2 / 2mL^2 \) where \( L \) = length of the box, \( h \) = reduced Planck’s constant, \( m \) = mass of the particle & \( n \) = Eigen values for energy.

Now as crystal size goes smaller to reach nano-regime,
means \( L \) is getting lowered, energy difference between highest occupied & lowest unoccupied states will be more. Thus more energy is required to fetch an electron from valence band to conduction band. Therefore, making single electron transport to occur to and from the nano-grain, more energy even greater than the available thermal energy is required.

III. SINGLE ELECTRON TRANSFER

Single electron transfer [2,5] phenomena hold due to unique coulomb blockade characteristics. Assuming quantum dot to be a initially electro-neutral metallic sphere, coulomb blockade can be explained vividly. Say, for the first time as one electron comes upon the sphere it delivers its full charge content to it making the sphere negatively charged and forming an electric field around it. Now as another electron proceeds towards the metallic dot, it gets strongly repelled by that existing field. Charge transfer in an ordinary conductor is continuous in manner and can be any valued due to large no. of free electron shift inside it. But if a highly resistive junction is placed there, it will surely restrict the free flow of charge carriers making them accumulate at one side of the junction. Fig.2 depicts that.

IV. CONCEPT OF CONTROLLED INVERTER

For subtraction of two binary numbers, 2’s complement of subtrahend is necessary. Here after making 1’s complement, 1 is added. In making this 1’s complement, Ex-or gate is used as a controlled inverter. If it is a two input Ex-or gate, one of the inputs is considered as control input another normal input. When, control input takes logic low value, output of the gate is same as the normal input. When it is logic high, output is complement of normal input provided.

V. PARALLEL ADDER/SUBTRACTOR CIRCUIT

For a four bit parallel adder/subtractor circuit, 4 controlled inverters are provided with one ADD/SUB control line along with four full adder circuits interconnected. When this control line is low valued, it makes simple addition of two four bit numbers. When it keeps higher logic, controlled inverters provide 1’s complement of addend. Thus 2’s complement is formed with addition of 1 to the above mentioned and when added to the other four bit data, subtraction happens. Thus same circuit is used as adder or subtractor.

VI. HYBRID SET-CMOS BASED 4-BIT PARALLEL ADDER/SUBTRACTOR CIRCUIT

Fig.3 reflects hybrid SET-CMOS based parallel adder/subtractor where \( Y_3, Y_2, Y_1, Y_0 \) & \( X_3, X_2, X_1, X_0 \) are added or subtracted to form output bits of \( S_3,S_2,S_1,S_0 \) & Cout.
VII. SIMULATION

Our design was simulated with the help of MIB and BSIM4.6.1 model & VDD was taken to be 0.7V at room temperature [4,7]. Parameters needed for our hybrid circuit are shown in table: 1.

Table: 1. Parameters taken for SET & PMOS

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>PARAMETER</th>
</tr>
</thead>
<tbody>
<tr>
<td>SET</td>
<td>(C_1=0.27aF, C_2=0.125aF, C_{GD}=C_{GS}=0.1aF, R_{TD}=R_{TS}=1M\Omega)</td>
</tr>
<tr>
<td>PMOS</td>
<td>(L=65\ nm, W=100\ nm); for other parameters standard values taken from model BSIM4.6.1</td>
</tr>
</tbody>
</table>

Fig.4 shows input voltage waveforms found at simulating the hybrid circuit and Fig.5 reflects the output responses we got accordingly.
VIII. POWER & PDP ANALYSIS

A noticeable reduction in power consumption is presented in comparison with so called CMOS logic over following table: 2.

Table: 2. Comparison of average power consumption

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conventional CMOS based Parallel Adder/Subtractor</th>
<th>Hybrid SET-CMOS based Parallel Adder/Subtractor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power consumption</td>
<td>3.77E-09 watts</td>
<td>6.05E-10 watts</td>
</tr>
</tbody>
</table>

Above comparison is graphically shown in fig. 6.

Power-delay product for conventional CMOS based circuit and its SET-CMOS based hybrid counterpart is tabled below in table: 3.

Table: 3. Power-delay product comparison

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conventional CMOS based Parallel Adder/Subtractor</th>
<th>Hybrid SET-CMOS based Parallel Adder/Subtractor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power-delay product</td>
<td>1.89E-16 Watt-sec.</td>
<td>3.3638E-17 Watt-sec.</td>
</tr>
</tbody>
</table>

Above comparison is graphically plotted below in fig. 7.

Fig.5: Output waveforms

Fig.6: Comparison of average power consumption

Fig.7: Power-delay product comparison
IX. CONCLUSION

Our designed room temperature operable hybrid SET-CMOS based [8] 4-bit Adder/Subtractor circuit shows considerable reduction in power consumption. As dynamic power comprises the maximum part of total power consumption (though in room temperature, leakage & short circuit power consumption occurs with non-minimum value), we have successfully reduced it by lowering the value of supply voltage VDD below 1V (as there is a quadratic dependence of switching power on VDD) as well as by making all island related capacitance values to lie within atto-farad range. Thus this paper presents another successful attempt in making feasibility for ultra dense circuit with ultra low power consumption in today’s nano-technological era.

IX. ACKNOWLEDGEMENT

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X. REFERENCE


Sudipta Mukherjee is currently working towards his M.Tech. degree in VLSI Design and Microelectronics Technology in the Department of Electronics and Telecommunication Engineering, Jadavpur University, Kolkata, India. His research areas are Hybrid Single Electron Transistor, DG-MOSFET, MODFET, CNTFET etc.

Tahesin Samira Delwar is a 3rd year student of the Department of EEE in the University of Science & Technology, Chittagong.

Anindya Jana is a PhD fellow in the Dept. of ETCE, Jadavpur University. Presently, he is working as an Assistant Professor in the Dept. of ETE at University of Science and Technology, Chittagong. He has more than 25 technical research papers in archived journals and peer-reviewed conferences. Recently his research initiatives are focused in the areas of simulations of nanodevice models, transport phenomenon, single-electron & spintronics devices and their applications in VLSI circuits, low power VLSI design.

Prof. Subir Kumar Sarkar is currently a Professor and the former HOD of the Department of Electronics and Telecommunication Engineering, Jadavpur University, Kolkata, India. He has published more than 450 technical research papers in archival International/National journals and peer-reviewed conferences and 4 Engineering text books in the field of Devices, Mobile ad hoc and Sensor Networks, Digital watermarking, RFID and its Applications.